wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode.

Please add new claims 42-45.

--42. A device according to claim 13,

wherein the semiconductor device comprises a CMOS transistor including the first thin film transistor and a second thin film transistor,

said second thin film transistor comprising:

a semiconductor island being formed on the insulating surface;

a channel region in the semiconductor island;

at least a fourth impurity region being formed in contact with the channel region of the second thin film transistor;

at least a fifth impurity region being formed in contact with the fourth impurity region;

a gate electrode of the second thin film transistor being formed over the charnel region with the gate insulating film being interposed therebetween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein each of the fourth and fifth impurity regions is overtapped with neither the third gate electrode nor the fourth gate electrode,

wherein the first thin film transistor is an n-channel thin film transistor while the second thin film, transistor is a p-channel thin film transistor.

43. A device according to claim 13,

wherein the semiconductor device comprises a CMOS transistor including the first thin film transistor and a second thin film transistor,

said second thin film transistor comprising:

a semiconductor island being formed on the insulating surface;

a channel region in the semiconductor island;

at least a fourth impurity region being formed in contact with the channel region;

a gate electrode of the second thin film transistor being formed over the channel

region with the gate insulating film being interposed therebetween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein the third gate electrode has at least a taper portion and a flat portion,

wherein the fourth impurity region is overlapped with neither the third gate electrode nor the fourth gate electrode,

wherein the first thin film transistor is an n-channel thin film transistor while the second thin film transistor is a p-channel thin film transistor.

44. A device according to claim 13,

wherein the semiconductor device comprises a CMOS transistor including the first thin film transistor and a second thin film transistor,

said second thin film transistor comprising:

a semiconductor island being formed on the insulating surface;

a channel region in the semiconductor island;

at least a fourth impurity region being formed in contact with the channel region;

a gate electrode of the second thin film transistor being formed over the channel region with the gate insulating film being interposed thereberween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein the fourth impurity region is overlapped with neither the third gate electrode nor the fourth gate electrode,

wherein the first thin film transistor is an n-channel thin film transistor while the second thin film transistor is a p-channel thin film transistor.

45. A device according to claim 13,

wherein the semiconductor device is electroluminescence display device, said electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion over a substrate;

at least the first thin film transistor for controlling a current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor being formed in the peripheral driving circuit portion;

a pixel electrode being electrically connected to the third impurity region of the

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first thin film transistor;

a light emitting layer being formed over the pixel electrode;

an electrode being formed over the light emitting layer.--